Gp/2826

Docket No. 740756-2138

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\ ^	THE UNITED STATES PATENT AND	TRAD	EMARK OFFICE		
In re P	atent Application of	)			
Takayuki IKEDA et al.		)	Examiner: Ahmed N. SEFER		
Serial No. 09/542,473		)		at the h	
Filed:	April 4, 2000	)	Group Art Unit: 2826	Teller	
For:	ELECTROOPTICAL DEVICE AND A METHOD	)	Confirmation No. 6069	HOODES	
	OF MANUFACTURING THE SAME	)		10 =25-02	
	Certificate of Mailing				
postage 2002	I hereby certify that this correspondence is being deposited with the as First Class Mail in an envelope addressed to Commissioner for P	e United Patents, W	States Postal Service with sufficient vashington, DC 20231, on Septembe	tr <u><b>2</b>5</u> ,	

SECOND REQUEST FOR ACKNOWLEDGMENT OF INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents Washington, D.C. 20231

Sir:

An Information Disclosure Statement with Form PTO-1449 was filed in the above identified patent application on September 4, 2001. Applicants have not yet received back from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the cited disclosed information.

The Examiner is requested to initial and return to the undersigned a copy of the subject Form PTO-1449.

Should there be any questions concerning this communication, please telephone the undersigned at the number set forth below.

Respectfully submitted

eff Costellia Registration No. 35,483

Nixon Peabody LLP 8180 Greensboro Drive, Suite 800 McLean, Virginia 22102 (703) 770-9300

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7-13	epartment of Commerce nt and Trademark Office	Atty Docket 0756-	Serial No. 09/542,473					
(Rev. 8-83) Patent  INFORMATION DISCLOSURE STA		Applicants: Takayuki IKEDA						
OF ICS		Filing Date: April 04, 2000		Group Art Unit: 2826				
act of the	U.S. PATENT	DOCUMENTS						
Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)			
6,013,929	01/11/2000	Ohtani						
отн	ER DOCUMENTS	(Including Author, Title, Date,	Pertinent Page	es, Etc.)				
Fabrication Method Thereof", F	iling Date: May 23,	1997, Inventor: Hisashi	OHTANI					
Specifications and Drawings for the Same, and Semiconductor	Application Serial N	lo. 09/468.859, "Thin Fil	m Transisto	r, Method of M 1999, Inventor	anufacturing Hisashi			
Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Device and Process for								
Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Device and Method of								
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			The state of the s	OCT -3 2002 TECHNOLOGY CENTER 2800	RECEIVED			
	Document Number 6,013,929  OTH  Specifications and Drawings for Fabrication Method Thereof", F Specifications and Drawings for the Same, and Semiconductor OHTANI Specifications and Drawings for Production Thereof" Filing Date Specifications and Drawings for Productions and Drawings for Production Thereof Productions and Drawings for Productions a	FORM THON DISCLOSURE STATEMENT  U.S. PATENT  Document Number  6,013,929  OTHER DOCUMENTS  Specifications and Drawings for Application Serial N Fabrication Method Thereof", Filing Date: May 23, Specifications and Drawings for Application Serial N the Same, and Semiconductor Device Including the OHTANI  Specifications and Drawings for Application Serial N Production Thereof" Filing Date: January 19, 2000, Specifications and Drawings for Application Serial N Production Thereof" Filing Date: January 19, 2000,	FORM THEN DISCLOSURE STATEMENT  Document Number  Filing Date: April 04, 26  U.S. PATENT DOCUMENTS  Document Number  OTHER DOCUMENTS  (Including Author, Title, Date, Patrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi Specifications and Drawings for Application Serial No. 08/862,895, "Semico Fabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi Specifications and Drawings for Application Serial No. 09/468,859, "Thin Fil the Same, and Semiconductor Device Including the Same" Filing Date: Decontrol of Thereof Filing Date: January 19, 2000, Inventors: Shunpei YA Specifications and Drawings for Application Serial No. 09/493,411, "Semicor Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YA Specifications and Drawings for Application Serial No. 09/493,411, "Semicor Production	FORMATION DISCLOSURE STATEMENT  Applicants: Takayuki IKEDA  Filing Date: April 04, 2000  U.S. PATENT DOCUMENTS  Document Number  Date  Name  Class  6,013,929  O1/11/2000  Othani  OTHER DOCUMENTS  (Including Author, Title, Date, Pertinent Page)  Specifications and Drawings for Application Serial No. 08/862,895, "Semiconductor Interfabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi OHTANI  Specifications and Drawings for Application Serial No. 09/468,859, "Thin Film Transistor the Same, and Semiconductor Device Including the Same" Filing Date: December 21, OHTANI  Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Deverous Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Fabricating the Same" Filing Date: January 28, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Deverous Theorems of Page 19, 2000, Inventors: Shunpei YAMAZAKI et as Specifications and Drawings for Appl	Applicants: Takayuki IKEDA  Filing Date: April 04, 2000 Group Art U  U.S. PATENT DOCUMENTS  Document Number Date Name Class Subclass  6,013,929 01/11/2000 Ohtani  OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)  Specifications and Drawings for Application Serial No. 08/862,895, "Semiconductor Intergrated Circuit Fabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi OHTANI  Specifications and Drawings for Application Serial No. 09/468,859, "Thin Film Transistor, Method of M the Same, and Semiconductor Device Including the Same" Filing Date: December 21, 1999, Inventor: OHTANI  Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Device and Proce-Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YAMAZAKI et al.			

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

Date Considered